CLAIMS

What is claimed is:

1. A contact for a semiconductor device, comprising:

a contact plug extending through a first barrier layer, wherein said contact plug is in electrical communication with an active region on a semiconductor substrate;

a contact land disposed upon said contact plug, wherein said contact land has a larger cross-sectional area than said contact plug;

an upper contact extending through a second barrier layer, which is disposed over said first barrier layer, to form an electrical contact with contact land.

2. A method of forming a contact for a semiconductor device, comprising:

providing a semiconductor substrate having at least one active region;

depositing a first barrier layer over said substrate;

forming a first opening through said first barrier layer to expose a portion of said at least one active region;

filling said first opening with a first conductive material to form a contact plug;

forming a conductive contact land over said contact plug;

depositing a second barrier layer over said first barrier layer and said conductive contact land;

forming a second opening through said second barrier layer to expose a portion of said conductive contact land; and

filling said second opening with a second conductive material to form said contact.

3. A bipolar transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further

including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least one active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through a first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through a first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

at least one drain contact land disposed atop said at least one drain contact plug, wherein said at least one drain contact land has a larger cross-sectional area than said at least one drain contact plug;

at least one source contact land disposed atop said at least one source contact plug, wherein said at least one source contact land has a larger cross-sectional area than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, wherein said at least one upper source contact is in electrical communication with said at least one source contact land; and

at least one upper drain contact extending through said second barrier layer, wherein said at least one upper drain contact is in electrical communication with said at least one drain contact land.

4. The bipolar transistor of claim 3, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

5. The bipolar transistor of claim 3, wherein said at least one source contact plug extends between at least two source regions.

6. The bipolar transistor of claim 3, wherein said at least one drain contact plug extends between at least two drain regions.

7. The bipolar transistor of claim 3, wherein said at least one source contact land extends between at least two source contact plugs.

8. The bipolar transistor of claim 3, wherein said at least one drain contact land extends between at least two drain contact plugs.

9. The bipolar transistor of claim 3, wherein said at least one upper source contact extends between at least two source contact lands.

10. The bipolar transistor of claim 3, wherein said at least one upper drain contact extends between at least two drain contact lands.

11. A method of producing a bipolar transistor for the dissipation of electrostatic discharges, comprising:

providing an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said drain region and said source region on said substrate active area;

depositing a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

planarizing said first barrier layer to expose said at least one gate member;

patterning a first etch mask on said first barrier layer, wherein said first resist layer includes openings substantially over said at least one drain region and over said at least one source region;

etching said first barrier layer to expose said at least one drain region and said at least one source region in said substrate forming at least one drain via and at least one source via, respectively;

removing said first etch mask;

depositing a layer of first conductive material over said first etched barrier layer to fill said at least one drain via and said at least one source via;

planarizing said first conductive material forming at least one drain contact plug and at least one source contact plug in said at least one drain via and said at least one source via, respectively;

patterning a first deposition material on said first buffer layer and said at least one transistor gate member, wherein said first deposition material includes openings over said at least one drain contact plug and said at least one source contact plug;

depositing a layer of second conductive material over said first deposition material to fill said openings over said at least one drain contact plug and said at least one source contact plug;

planarizing said second conductive material to said first deposition material to form at least one drain contact land and at least one source contact land;

removing said first deposition material;

depositing a second barrier layer over said first barrier layer and said at least one drain contact land and at least one source contact land;

patterning a second etch mask on said second barrier layer, wherein said second resist layer includes openings substantially over said at least one drain contact land and over said at least one source contact land;

etching said second barrier layer to expose said at least one drain contact land and said at least one source contact land forming at least one drain contact via and at least one source drain via, respectively;

removing said second etch mask;

depositing a layer of third conductive material over said etched second barrier layer to fill said at least one drain contact via and said at least one source contact via; and

planarizing said third conductive material forming at least one upper drain contact and at least one upper source contact in said at least one drain contact via and said at least one source contact via, respectively.

12. The method of claim 11, further comprising:

patterning a second deposition material on said second buffer layer, said at least one upper drain contact, and said at least one upper source contact, wherein said first deposition material includes openings over said at least one upper drain contact and said at least one upper source contact;

depositing a layer of fourth conductive material over said second deposition material to fill said openings over said upper drain contact and said upper source contact;

planarizing said fourth conductive material to said second deposition material to form a drain contact metallization and a source contact metallization; and

removing said second deposition material.

13. The method of claim 11, wherein said at least one source contact plug extends between at least two source regions.

14. The method of claim 11, wherein said at least one drain contact plug extends between at least two drain regions.

15. The method of claim 11, wherein said at least one source contact land extends between at least two source contact plugs.

16. The method of claim 11, wherein said at least one drain contact land extends between at least two drain contact plugs.

17. The method of claim 11, wherein said at least one upper source contact extends between at least two source contact lands.

18. The method of claim 11, wherein said at least one upper drain contact extends between at least two drain contact lands.

19. A semiconductor device including at least one contact, comprising:
a contact plug extending through a first barrier layer, wherein said contact plug is in electrical communication with an active region on a semiconductor substrate;
a contact land disposed atop said contact plug, wherein said contact land has a larger cross-sectional area than said contact plug;
an upper contact extending through a second barrier layer, which is disposed over said first barrier layer, to form an electrical contact with contact land.

20. A method of forming a semiconductor device having at least one contact, comprising:
providing a semiconductor substrate having at least one active region;
depositing a first barrier layer over said substrate;
forming a first opening through said first barrier layer to expose a portion of said at least one active region;
filling said first opening with a first conductive material to form a contact plug;
forming a conductive contact land over said contact plug;

depositing a second barrier layer over said first barrier layer and said conductive contact land;

forming a second opening through said second barrier layer to expose a portion of said conductive contact land; and

filling said second opening with a second conductive material to form said contact.

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21. A semiconductor device including at least one bipolar transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through a first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through a first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least source region on said semiconductor substrate;

at least one drain contact land disposed atop said at least one drain contact plug, wherein said at least one drain contact land has a larger cross-sectional area than said at least one drain contact plug;

at least one source contact land disposed atop said at least one source contact plug, wherein said at least one source contact land has a larger cross-sectional area than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, wherein said at least one upper source contact is in electrical communication with said at least one source contact land; and

at least one upper drain contact extending through said second barrier layer, wherein said at least one upper drain contact is in electrical communication with said at least one drain contact land.

22. The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

23. The semiconductor device of claim 21, wherein said at least one source contact plug extends between at least two source regions.

24. The semiconductor device of claim 21, wherein said at least one drain contact plug extends between at least two drain regions.

25. The semiconductor device of claim 21, wherein said at least one source contact land extends between at least two source contact plugs.

26. The semiconductor device of claim 21, wherein said at least one drain contact land extends between at least two drain contact plugs.

27. The semiconductor device of claim 21, wherein said at least one upper source contact extends between at least two source contact lands.

28. The bipolar transistor of claim 21, wherein said upper drain contact extends between at least two drain contact lands.